



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/736,061	12/15/2003	Christopher Olsen	AMAT/8629/FEP/GCM/RKK	4253

7590 02/13/2006

PATENT COUNSEL
APPLIED MATERIALS, INC.
Legal Affairs Department
P.O. Box 450A
Santa Clara, CA 95052

EXAMINER

SELLMAN, CACHET I

ART UNIT	PAPER NUMBER
----------	--------------

1762

DATE MAILED: 02/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/736,061	Applicant(s) OLSEN ET AL.	
	Examiner Cachet I. Sellman	Art Unit 1762	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 15 December 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-26 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-26 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>07/25/2005</u> , <u>3/15/2004</u> | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:
 - I. Claims 1-18, drawn to a method, classified in class 427, subclass 569.
 - II. Claims 19-26, drawn to a product, classified in class 438, subclass 1+.

The inventions are distinct, each from the other because of the following reasons:

2. Inventions I and II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case the SiOxNy film can be made using a materially different process such as a sputtering process.
3. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.
4. During a telephone conversation with B. Todd Patterson on January 20, 2006 a provisional election was made with traverse to prosecute the invention of Group 1, claims 1-18. Affirmation of this election must be made by applicant in replying to this Office action. Claim 19-26 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.
5. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one

Art Unit: 1762

or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Specification

6. The disclosure is objected to because of the following informalities: In paragraph 0031 it states "load locks 102 or 104" this seems to be a typographical error and should read load locks 104 or 106. In paragraph 0033 it says "load locks 302 or 304" it should read load lock 304 or 306.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1 the applicant claims forming a SiO_xN_y gate dielectric but does not define x or y in the claim therefore it is not clear as to what type of gate dielectric is being formed.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

10. Claims 1-3, 5, and 7-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Cheng et al. (US 6649538).

Cheng et al. discloses a method for forming a nitrided gate oxide on a silicon substrate by first forming a silicon dioxide layer over the silicon substrate (abstract); followed by a nitriding annealing process in an ambient including NH₃ (column 4, lines 39-42); and then exposing the gate oxide to a plasma nitriding treatment comprising a nitrogen source (column 4, lines 56-63 and column 5, lines 7-10) as required by **claim 1**. The method includes the step of annealing the structure after exposing it to the plasma (column 6, lines 10 – 30) as required by **claim 2**. The annealing can be performed in an oxygen containing atmosphere (column 6, lines 10-15, 19, and 22) as required by **claim 3**. The nitrogen source in the plasma nitriding treatment is N₂ (column 5, lines 7-8) as required by **claim 5**. The substrate is exposed to plasma at a pressure of 1milliTorr to about 50 milliTorr (column 5, lines 2-5) as required by **claim 7**.

Art Unit: 1762

The silicon dioxide layer can be formed by oxidizing a top surface of the silicon substrate (column 4, lines 14-26) as required by **claim 8**. Heating the structure in a NH_3 atmosphere nitrates the structure without incorporating oxygen (column 4, lines 41-42) as required by **claims 9**.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

12. Claims 10-12, 14, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheng et al. as applied to claims 1-3, 5, and 7-9 stated above in view of Kiryu et al. (US 2004/0053472 A1).

The teachings of Cheng et al. as applied to claims 1-3, 5, and 7-9 are as stated above.

Cheng et al. does not teach using an integrated system to form the SiO_xN_y where the structure is heated in a NH_3 atmosphere in a first processing chamber then transferred to a second chamber where it is exposed to a plasma as required by **claim 10**.

Kiryu et al. discloses an apparatus for film formation of a gate insulator, which enables the formation of a gate of a high dielectric constant material using a cluster tool [0005]. The cluster tool performs various kinds of processes for an object such as film forming, annealing and removal of natural oxide film [0134]. The tool consists of processing chambers in which various processes can be performed a transfer chamber, load lock chamber, and a transfer arm that delivers the object to each processing chamber and once the film is formed the substrate is removed from the processing chamber. Using the cluster tool to form a gate insulator prevents contamination of the object by the atmosphere. When this apparatus is used for film formation of a gate insulator the process can be carried out successively with low burden [0143].

It would have been obvious to one having ordinary skill in the art at the time the invention was made to perform the process taught by Cheng et al. in the apparatus of Kiryu et al. where a first processing chamber is used for heating the substrate in an NH_3 atmosphere; a second chamber is used for exposing the substrate to a plasma containing a nitrogen source. One would have been motivated to do so because Cheng et al. discloses a method for forming a high dielectric constant gate insulator (SiO_xN_y) and Kiryu et al. teaches that the apparatus can be used to form a high dielectric constant gate insulator such as SiO_xN_y using a substrate that has a layer of silicon dioxide [0014] where the insulator is not contaminated by the atmosphere and is formed with low burden and Kiryu et al. further states that the processing chambers of the apparatus can be used to perform the processes that are used by Cheng et al. to form

the film (such as annealing and film forming) therefore one would have a reasonable expectation of success in forming the SiO_xN_y film without contamination of the film as well as with low burden.

Cheng et al. further teaches the step of annealing the substrate after exposing it to plasma (column 6, lines 10-30). Therefore it would have been obvious to transfer the substrate to a third processing chamber in order to perform the annealing step as required by **claim 11**. Cheng et al. discloses annealing the substrate in an atmosphere of O_2 (column 6, lines 10-15, 19, 22) as required by **claim 16**. Cheng et al. teaches that the silicon dioxide film is formed by oxidation (column 4, lines 14-26) and Kiryu et al. discloses that the processing chambers of the apparatus can be used for film forming and that a silicon dioxide layer is formed first before the formation of the SiO_xN_y film [0014] therefore it would have been obvious to have a processing chamber for forming the silicon dioxide layer as required by **claims 12 and 14**.

13. Claims 4 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheng et al. in view of Kiryu et al. as applied to claims 1 and 16 above in view of Niimi et al. (US 6548366 B2).

The teachings of Cheng et al. in view of Kiryu et al. as applied to claims 1 and 16 are as stated above.

Cheng et al. in view of Kiryu et al. does not teach annealing the structure in an inert or reducing atmosphere before annealing in an atmosphere comprising O₂ as required by **claims 4 and 17**.

Niimi et al. discloses a method of two step annealing a silicon dioxide layer to form an uniform nitrogen profile within the layer. In the method disclosed a silicon dioxide layer is exposed to a nitrogen – containing plasma and reoxidized and annealed to stabilize the nitrogen distribution, heal plasma-induced damage and reduce interfacial defect density (abstract). The annealing and re-oxidation step consists of annealing the structure in a mixture of H₂ and N₂ gas then annealing it in a mixture of O₂ and N₂ gas to heal plasma-induced damage after nitrogen containing plasma exposure. Niimi et al. further discloses that these two steps are executed consecutively without substantial delay between them (column 6, lines 14-35).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the process taught by Cheng et al. to include the step of annealing the structure in an inert atmosphere before annealing in an atmosphere of O₂. One would have been motivated to do so because both Cheng et al. and Niimi et al. disclose processes for forming an SiO_xN_y film that include using a silicon substrate with a silicon oxide film; exposing it to a plasma with a nitrogen source; and annealing in an oxygen atmosphere and Niimi et al. further discloses that by annealing in an inert atmosphere then in an atmosphere of O₂ heals plasma-induced damage as well as

Art Unit: 1762

stabilize the nitrogen distribution in the film therefore one would have a reasonable expectation of success in forming the SiO_xN_y film with stabilized nitrogen distribution and that is healed from the damage induced by plasma.

14. Claims 6 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheng et al. in view of Kiryu as applied to claims 1 and 10 above, and further in view of Ibok (US 2001/0049186).

The teachings of Cheng et al. in view of Kiryu et al. as applied to claims 1 and 10 are stated above.

Cheng et al. in view of Kiryu et al. does not disclose heating the substrate in an atmosphere of NH_3 at a temperature of at least 700°C and at a pressure less than about 100 Torr as required by **claim 6** or placing the substrate in a cooling chamber after heating and before exposing it to a plasma as required by **claim 18**.

Ibok discloses a method for making a gate insulator on a silicon substrate, which includes the steps of forming a thin oxide film on the substrate then annealing the substrate in ammonia at a temperature up to 1100°C (abstract and [0017]).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the process of Cheng et al. in view of Kiryu et al. by heating the substrate at the temperatures disclosed by Ibok. One would have been

Art Unit: 1762

motivated to do so because Cheng et al. in view of Kiryu et al. disclose a method for forming a gate insulator by heating a silicon substrate with a silicon oxide layer thereon in an atmosphere of NH_3 to incorporate nitrogen in to the film but does not teach the annealing temperature and Ibok also teaches the same process with the goal of establishing a nitrogen concentration within the film [0017] therefore one would have a reasonable expectation of success in forming the SiO_xN_y film.

The pressure limitation is not taught by Cheng et al. discloses that the plasma process occurs at a pressure of about 1 milliTorr to about 100 milliTorr (column 4, lines 61-63). One would have been motivated to heat the substrate at these pressures in order to use the same processing chamber for two steps, which would result in less time to form the SiO_xN_y layer.

In regards to **claim 18**, where the applicant requires the use of a cool down chamber after heating and before transferring to a second processing chamber, It would have been obvious to one having ordinary skill in the art to include a cool down chamber when going from a heating step where the temperature can get up to 1100°C to a step where the substrate is being exposed to a plasma at a temperature of about $300 - 400^\circ\text{C}$ (Cheng et al. column 4, lines 64 - column 5, lines 1-5).

Art Unit: 1762

15. Claims 13 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheng et al. in view of Kiryu et al. as applied to claims 1 and 19 above, and further in view of Burnham et al. (US 6649538 B1).

The teachings of Cheng et al. in view of Kiryu et al. as applied to claims 1 and 19 are as stated above.

Cheng et al. in view of Kiryu et al. does not disclose forming a polysilicon layer on the substrate as required by claims **13 and 15**.

Burnham et al. discloses a method for forming a MOSFET transistor, which includes a silicon substrate, and a polysilicon gate formed on top of a thin gate dielectric layer where the thin gate dielectric layer is silicon oxynitride (column 1, lines 17-25).

It would have been obvious to one having ordinary skill at the time the invention was made to modify the process taught by Cheng et al. in view of Kiryu et al. to include the step of forming a polysilicon gate layer on top of the silicon oxynitride. One would have been motivated to do so because Cheng et al. discloses that this process of forming a SiO_xN_y film can be used for a MOSFET where a gate electrode is formed over a gate dielectric and Burnham et al. teaches that the polysilicon (gate electrode) can be formed over a thin gate dielectric layer (SiO_xN_y) therefore one would have a reasonable expectation of success in forming the MOSFET.

In regards to **claim 15**, where the applicant requires that the substrate is transferred to a fifth processing chamber that is external to the integrated processing system where the polysilicon layer is deposited, it would have been obvious to one having ordinary skill in the art that to transfer the substrate to another processing chamber because Kiryu et al. discloses that the substrate can be removed from the process after the formation of the gate electrode (SiO_xN_y).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cachet I. Sellman whose telephone number is 571-272-0691. The examiner can normally be reached on Monday through Friday, 7:00 - 4:30pm.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Meeks can be reached on 571-272-1423. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Application/Control Number: 10/736,061
Art Unit: 1762

Page 13

Cachet Sellman
Patent Examiner
Art Unit 1762



TIMOTHY MEEKS
SUPERVISORY PATENT EXAMINER